AMENDMENTS TO THE CLAIMS

Please cancel claims 5, 17 and 20 without prejudice. Please add claim 21.

1. (CURRENTLY AMENDED) A circuit comprising:

a register stack configured as (i) a plurality of segments addressable through a segment address signal and (ii) a plurality of registers within each of said plurality of segments, said plurality of registers being addressable through a register address signal;

a control circuit connected to said register stack and configured to (i) store a plurality of register states, and (ii) store a segment count signal, ~~and (iii) present said segment address signal responsive to said register states, said segment count signal, and said register address signal~~ wherein said control circuit comprises (A) a status circuit configured to present a gating signal responsive to both said register address signal and said register states and (B) a plurality of logic gates configured to present said segment address signal by logically ANDing said gating signal and said segment count signal; and

a ~~state~~ stack register connected to said control circuit and configured to present said register states to said control circuit, wherein each of said register states has one associated register of said registers.

2. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein at least one of said register states is fixed in a global state indicating that data cannot be pushed onto said one associated register.

3. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein at least one of said register states is fixed in a stackable state indicating that data can be pushed onto said one associated register.

4. (CURRENTLY AMENDED) The circuit according to claim 1, wherein said register stack further comprises:

a first portion disposed within a processor and configured as at least one segment of said plurality of segments~~;~~ ~~and~~

~~a second portion disposed external to said processor and configured as at least one segment of said plurality of segments~~.

5. (CANCELED)

6. (CURRENTLY AMENDED) The circuit according to claim ~~5~~ 1, wherein said status circuit comprises:

a comparator configured to present said gating signal by comparing said register states and said register address signal.

7. (CURRENTLY AMENDED) The circuit according to claim ~~5~~ 1, wherein said status circuit comprises:

a memory device configured to (i) store said register states and (ii) present said gating signal by reading out one of said register states as addressed by said register address signal.

8. (CURRENTLY AMENDED) The circuit according to claim ~~17~~ 1, wherein said plurality of logic gates are further configured to present said segment address signal as a predetermined address responsive to said gating signal having a global state.

9. (PREVIOUSLY PRESENTED) The circuit according to claim 8, wherein said status circuit comprises:

a comparator configured to present said gating signal by comparing said register states and said register address signal.

10. (CURRENTLY AMENDED) A method of controlling a register stack comprising the steps of:

(A) presenting a plurality of register states from a stack register, wherein each of said register states has one associated register of a plurality of registers in said register stack;

(B) storing said register states presented from said stack register;

(C) storing a segment count;

~~(A)~~ (D) presenting a gating signal responsive to both ~~comparing~~ a register address ~~with a plurality of~~ and said register states ~~to present a gating signal~~;

~~(B)~~ (E) logically ANDing said ~~gating a~~ segment count with said gating signal to present a segment address;

~~(C)~~ (F) addressing a plurality of segments within said register stack with said segment address; and

~~(D)~~ (G) addressing said registers within one of said segments with said register address.

11. (CURRENTLY AMENDED) The method according to claim 10, wherein step ~~(A)~~ (D) further comprises the ~~sub-steps~~ sub-step of:

~~presenting a signal communicating said plurality of register states; and~~

selecting one of said plurality of register states as said gating signal based upon said register address.

12. (PREVIOUSLY PRESENTED) The method according to claim 10, further comprising the step of:

writing said plurality of register states into a register under software control in response to a reset handler operation for a processor executing said software.

13. (ORIGINAL) The method according to claim 10, further comprising the step of:

incrementing said segment address in response to a push instruction.

14. (CURRENTLY AMENDED) The method according to claim ~~13~~ 10, further comprising the step of:

decrementing said segment address in response to a pop instruction.

15. (CURRENTLY AMENDED) A circuit comprising:

register stack means configured as (i) a plurality of segments addressable through a segment address and (ii) a plurality of registers within each of said plurality of segments, said plurality of registers being addressable through a register address;

means for storing a plurality of register states;

means for storing a segment count;

means for presenting a gating signal responsive to both said register address and said register states;

means for presenting said segment address by logically ANDing ~~responsive to said register address and said plurality of register states~~ said gating signal and said segment count; and

means for ~~present~~ presenting said register states to said means for storing said register states, wherein each of said register states has one associated register of said registers.

16. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said control circuit comprises:

a counter configured to present said segment count signal identifying a current segment of said segments at a logical top of said register stack.

17. (CANCELED)

18. (PREVIOUSLY PRESENTED) The method according to claim 10, further comprising the step of:

presenting said segment address as a predetermined address responsive to said gating signal having a global state.

19. (CURRENTLY AMENDED) The method according to claim 10, ~~comprises~~ further comprising the step of:

transferring said register states from a first memory to a second memory ~~prior to said comparing~~.

20. (CANCELED)

21. (NEW) The circuit according to claim 4, wherein said register stack further comprises:

a second portion disposed external to said processor and configured as at least one segment of said plurality of segments.